IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of: **BRADLEY NELSON ET AL.**	§	Attorney Docket No. **AUS920030119US1**
Serial No.: **10/750,590**	§	Examiner: **SILVER, DAVID**
Filed: **12/31/2003**	§	Art Unit: **2128**
For: **METHOD, SYSTEM AND PROGRAM PRODUCT SUPPORTING USER TRACING IN A SIMULATOR**	§	Confirmation No.: **8597**

APPEAL BRIEF UNDER 37 C.F.R. 41.37

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Sir:

This Appeal Brief is submitted in support of the Appeal of the Examiner's final rejection of the claims in the above-identified application.

REAL PARTY IN INTEREST

The real party in interest in the present Appeal is International Business Machines Corporation, the Assignee of the present application.

RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellants, the Appellants' legal representative, or assignee, which directly affect or would be directly affected by or have a bearing on the Board's decision in the pending Appeal.

STATUS OF CLAIMS

Claims 1-45 were originally presented. Claims 46-87 have been entered during prosecution, and Claims 1-11, 13-26, 28-41, 43-51, 53, 60-65, 67, 74-79 and 81 have been canceled. Thus, Claims 12, 27, 42, 52, 54-59, 66, 68-73, 80 and 82-87 remain pending and stand finally rejected by the Examiner as noted in the Final Office Action dated July 3, 2008. The rejection of each pending claim is appealed.

STATUS OF AMENDMENTS

Four Amendments, entitled Amendment A, Amendment B, Amendment C and Amendment D, were entered during prosecution. No amendment has been submitted or entered subsequent to the Final Office Action dated July 3, 2008.

SUMMARY OF CLAIMED SUBJECT MATTER

Independent Claim 12 recites a method of reporting simulation data obtained by the simulation of an electronic design within a data processing system (see, e.g., Figures 1-2; page 9, line 1 *et seq.*). The method includes a simulator running a testcase against a simulation model of the electronic design (see, e.g., Figure 15, block 1504; page 68, line 16 *et seq.*). The simulation model is formed of representations of instances of a plurality of design entities (see, e.g., Figure 3A, reference numeral 300; page 11, line 17 *et seq.*), where the instances of the design entities contain a plurality of signals and functional logic that define functional operation of the electronic design (page 11, line 17 through page 12, line 20). Each instance of at least a particular design entity of the plurality of design entities contains an instance of an instrumentation entity that monitors the containing instance of the particular design entity but

does not contribute to functional operation of the electronic design (see, e.g., Figure 13, reference numerals 1314a and 1314b; page 64, line 21 through page 65, line 2). Each instance of the instrumentation entity contains a trace array (see, e.g., Figures 13-14, trace array 1320; page 65, line 4 *et seq.*) logically coupled to receive a monitored signal set including at least one signal among the plurality of signals (see, e.g., Figure 13; page 65, line 4 *et seq.*), where the trace array is further logically coupled to receive a control signal among the plurality of signals (see, e.g., Figure 13, CTRL signal; page 65, line 12 *et seq.*). With the trace array, trace data for the monitored signal set is recorded during the running of the testcase, where the recording includes concurrently storing within the trace array multiple values of the monitored signal set obtained over multiple cycles of functional operation of the simulation model (see, e.g., Figure 14, entries 1402a-1402n; page 66, line 28 *et seq.*). Values assumed by the monitored signal set are recorded in the trace array for only those cycles of functional operation during which the control signal is asserted so that no values assumed by the monitored signal set are recorded for those cycles of functional operation during which the control signal is not asserted (see, e.g., page 66, lines 21-23). A number of functional cycles elapsed between the values assumed by the monitored signal set are also recorded within the trace array (see, e.g., Figure 14, count field 1408; page 67, line 12 *et seq.*). The trace data is exported from the trace array in a trace file, and the trace file is stored in data storage (see, e.g., Figure 15, block 1512; page 69, line 4 *et seq.*).

Independent Claim 27 recites a data processing system (see, e.g., Figures 1-2; page 9, line 1 *et seq.*) including a number of elements recited in the format permitted by 35 U.S.C. § 112, paragraph six. The data processing system includes means for running a testcase against a simulation model of an electronic design (see, e.g., Figure 15, block 1504; page 68, line 16 *et seq.*). The simulation model is formed of representations of instances of a plurality of design entities (see, e.g., Figure 3A, reference numeral 300; page 11, line 17 *et seq.*), where the instances of the design entities contain a plurality of signals and functional logic that define functional operation of the electronic design (page 11, line 17 through page 12, line 20). Each instance of at least a particular design entity of the plurality of design entities contains an instance of an instrumentation entity that monitors the containing instance of the particular design entity but does not contribute to functional operation of the electronic design (see, e.g., Figure 13, reference numerals 1314a and 1314b; page 64, line 21 through page 65, line 2). Each

instance of the instrumentation entity contains a trace array (see, e.g., Figures 13-14, trace array 1320; page 65, line 4 *et seq.*) logically coupled to receive a monitored signal set including at least one signal among the plurality of signals (see, e.g., Figure 13; page 65, line 4 *et seq.*), where the trace array is further logically coupled to receive a control signal among the plurality of signals (see, e.g., Figure 13, CTRL signal; page 65, line 12 *et seq.*). The data processing system further includes means for recording trace data for the monitored signal set within the trace array during the running of the testcase, where the recording includes concurrently storing within the trace array multiple values of the monitored signal set obtained over multiple cycles of functional operation of the simulation model (see, e.g., Figure 14, entries 1402a-1402n; page 66, line 28 *et seq.*). The means for recording trace data includes means for recording, within the trace array, values assumed by the monitored signal set during only those cycles of functional operation during which the control signal is asserted and for refraining from recording values assumed by the monitored signal set during those cycles of functional operation during which the control signal is not asserted, such that no values assumed by the monitored signal set are recorded for those cycles of functional operation during which the control signal is not asserted (see, e.g., page 66, lines 21-23). The means for recording also includes means for recording in the trace array a number of functional cycles elapsed between the values assumed by the monitored signal set (see, e.g., Figure 14, count field 1408; page 67, line 12 *et seq.*). The data processing system further includes means for exporting the trace data from the trace array in a trace file and storing the trace file in data storage (see, e.g., Figure 15, block 1512; page 69, line 4 *et seq.*).

Independent Claim 42 recites an apparatus including a computer usable medium containing program code (see, e.g., page 75, line 26 *et seq.*). The program code includes instructions for running a testcase against a simulation model of an electronic design (see, e.g., Figure 15, block 1504; page 68, line 16 *et seq.*). The simulation model is formed of representations of instances of a plurality of design entities (see, e.g., Figure 3A, reference numeral 300; page 11, line 17 *et seq.*), where the instances of the design entities contain a plurality of signals and functional logic that define functional operation of the electronic design (page 11, line 17 through page 12, line 20). Each instance of at least a particular design entity of the plurality of design entities contains an instance of an instrumentation entity that monitors the

containing instance of the particular design entity but does not contribute to functional operation of the electronic design (see, e.g., Figure 13, reference numerals 1314a and 1314b; page 64, line 21 through page 65, line 2). Each instance of the instrumentation entity contains a trace array logically coupled to receive a monitored signal set including at least one signal among the plurality of signals (see, e.g., Figure 13; page 65, line 4 *et seq.*), wherein the trace array is further logically coupled to receive a control signal among the plurality of signals (see, e.g., Figure 13, CTRL signal; page 65, line 12 *et seq.*). The program code includes instructions for recording trace data for the monitored signal set within the trace array during the running of the testcase, where the recording includes concurrently storing within the trace array multiple values of the monitored signal set obtained over multiple cycles of functional operation of the simulation model (see, e.g., Figure 14, entries 1402a-1402n; page 66, line 28 *et seq.*). The instructions for recording trace data include instructions for recording, within the trace array, values assumed by the monitored signal set during only those cycles of functional operation during which the control signal is asserted and for refraining from recording values assumed by the monitored signal set during those cycles of functional operation during which the control signal is not asserted, such that no values assumed by the monitored signal set are recorded for those cycles of functional operation during which the control signal is not asserted (see, e.g., page 66, lines 21-23). The instructions for recording also including instructions for recording in the trace array a number of functional cycles elapsed between the values assumed by the monitored signal set (see, e.g., Figure 14, count field 1408; page 67, line 12 *et seq.*). The program code further includes instructions for exporting the trace data from the trace array in a trace file and storing the trace file in data storage (see, e.g., Figure 15, block 1512; page 69, line 4 *et seq.*).

In addition to the features of Claim 12, dependent Claim 52 recites that exporting the trace data in a trace file includes exporting the trace data in a trace file indicating an association between a value of the monitored signal set and an enumerated value containing a textual string (see, e.g., Figure 16, enum map 1608; page 69, line 22 *et seq.*).

In addition to the features of Claim 12, dependent Claim 54 recites that the trace array has a counter that counts the functional cycles and recording trace data includes recording in the

trace array an entry indicating overflow of the counter (see, e.g., Figure 14, overflow field 1404; page 67, line 16 *et seq.*).

In addition to the features of Claim 12, dependent Claim 56 recites that the exporting includes exporting a trace file including a plurality of fields, where the plurality of fields include at least one of a set comprising a file version field and an array type field indicating one of plurality of trace array types (see, e.g., Figure 16, version field 1602 and array type field 1604; page 69, line 15 *et seq.*).

In addition to the features of Claim 12, dependent Claim 57 recites that the storing includes grouping all trace files from for each of a plurality of simulation runs in a respective one of a plurality of file system subdirectories that are each dedicated to one of the plurality of simulation runs (see, e.g., Figure 17, non-volatile storage 1704; page 70, line 15 *et seq.*).

In addition to the features of Claim 12, dependent Claim 58 recites automatically naming the trace file in data storage by a filename indicating the containing instance of the particular design entity (see, e.g., Figure 17, trace files 1600; page 70, line 12 *et seq.*).

In addition to the features of Claim 27, dependent Claim 66 recites that the means for exporting the trace data in a trace file includes means for exporting the trace data in a trace file indicating an association between a value of the monitored signal set and an enumerated value containing a textual string (see, e.g., Figure 16, enum map 1608; page 69, line 22 *et seq.*).

In addition to the features of Claim 27, dependent Claim 68 recites that the trace array has a counter that counts the functional cycles and the means for recording trace data includes means for recording in the trace array an entry indicating overflow of the counter (see, e.g., Figure 14, overflow field 1404; page 67, line 16 *et seq.*).

In addition to the features of Claim 27, dependent Claim 70 recites that the means for exporting includes means for exporting a trace file including a plurality of fields, the plurality of fields including at least one of a set comprising a file version field and an array type field

indicating one of plurality of trace array types (see, e.g., Figure 16, version field 1602 and array type field 1604; page 69, line 15 *et seq.*).

In addition to the features of Claim 27, dependent Claim 71 recites that the means for storing comprises means, for each of a plurality of simulation runs, for grouping all trace files from that simulation run in a respective one of a plurality of file system subdirectories that are each dedicated to one of the plurality of simulation runs (see, e.g., Figure 17, non-volatile storage 1704; page 70, line 15 *et seq.*).

In addition to the features of Claim 27, dependent Claim 72 recites that the means for storing comprises means for automatically naming the trace file in data storage by a filename indicating the containing instance of the particular design entity (see, e.g., Figure 17, trace files 1600; page 70, line 12 *et seq.*).

In addition to the features of Claim 42, dependent Claim 80 recites that the instructions for exporting the trace data in a trace file include instructions for exporting the trace data in a trace file indicating an association between a value of the monitored signal set and an enumerated value containing a textual string (see, e.g., Figure 16, enum map 1608; page 69, line 22 *et seq.*).

In addition to the features of Claim 42, dependent Claim 82 recites that the trace array has a counter that counts the functional cycles and the instructions for recording trace data include instructions for recording in the trace array an entry indicating overflow of the counter (see, e.g., Figure 14, overflow field 1404; page 67, line 16 *et seq.*).

In addition to the features of Claim 42, dependent Claim 84 recites that the instructions for exporting include instructions for exporting a trace file including a plurality of fields, where the plurality of fields include at least one of a set comprising a file version field and an array type field indicating one of plurality of trace array types (see, e.g., Figure 16, version field 1602 and array type field 1604; page 69, line 15 *et seq.*).

In addition to the features of Claim 42, dependent Claim 85 recites that the instructions for storing comprise instructions that, for each of a plurality of simulation runs, group all trace files from that simulation run in a respective one of a plurality of file system subdirectories that are each dedicated to one of the plurality of simulation runs (see, e.g., Figure 17, non-volatile storage 1704; page 70, line 15 *et seq.*).

In addition to the features of Claim 42, dependent Claim 86 recites that the instructions for storing comprises instructions for automatically naming the trace file in data storage by a filename indicating the containing instance of the particular design entity (see, e.g., Figure 17, trace files 1600; page 70, line 12 *et seq.*).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. The final rejection of Claims 12, 27, 42, 52-55, 57-58, 66-73 and 80-87 under 35 U.S.C. 103(a) as unpatentable over U.S. Patent No. 5,604,895 to *Raimi* in view of U.S. Patent No. 4,821,178 to *Levin et al.* (*Levin*) set forth in paragraph 7 of the Final Office Action;
2. The final rejection of Claims 56, 58, 70, 72, 84 and 86 under 35 U.S.C. 103(a) as unpatentable over *Raimi* in view of *Levin* and further in view of the Examiner's Official Notice set forth in paragraph 9 of the Final Office Action; and
3. The final rejection of Claims 57, 71 and 85 under 35 U.S.C. 103(a) as unpatentable over *Raimi* in view of *Levin* and further in view of U.S. Publication No. 2003/0158871 to *Fomenko* set forth in paragraph 10 of the Final Office Action.

ARGUMENT

I. REJECTION OF CLAIMS 12, 27, 42, 52-55, 57-58, 66-73 AND 80-87 UNDER 35 U.S.C. § 103

In paragraph 7 of the Final Office Action, Claims 12, 27, 42, 52-55, 57-58, 66-73 and 80-87 stand finally rejected under 35 U.S.C. 103(a) as unpatentable over U.S. Patent No. 5,604,895 to *Raimi* in view of U.S. Patent No. 4,821,178 to *Levin et al.* (*Levin*). That rejection is not well founded and should be reversed.

A. Combination of *Raimi* and *Levin* does not disclose "recording ... a number of functional cycles elapsed between said values assumed by the monitored signal set" as recited in exemplary independent Claim 12

The final rejection of exemplary Claim 12 under 35 U.S.C. § 103 should be reversed because the combination of *Raimi* and *Levin* does not disclose each feature of exemplary Claim 12. For example, the cited combination of references does not disclose:

> recording trace data for the monitored signal set within the trace array during the running of the testcase ... , wherein recording trace data includes ... recording within the trace array a number of functional cycles elapsed between said values assumed by the monitored signal set. [Emphasis supplied]

With reference to this feature, page 4 of the Final Office Action cites col. 26, line 58 through col. 27, line 4 of *Raimi*. The cited passage discloses:

> Separate trak_file output files are available for each test case simulated. These trak_files detail the extent to which a particular test case covers events tracked in each HDL file simulated. The task of a test reduction algorithm or program would be to examine these trak_files, and to find a minimal subset of tests such that certain predetermined coverage goals are met. These constraints could be set out more precisely as: x % execution check coverage, y % dead-logic coverage, z % behavioral-controllability coverage, or z % of any other type of check run, and a total run time (in simulation clocks) under t clocks. The task of the program would be to find the subset of tests which gave the greatest coverage percentages, while not exceeding the total clock limit. [Emphasis supplied]

With respect to claimed feature, the cited passage of *Raimi* in combination with *Levin* discloses that the post-simulation analysis performed by a test reduction algorithm can set as a constraint a total run time in terms of simulation clocks. The cited teaching of the combination of *Raimi* and *Levin* does not disclose "recording ... a number of functional cycles elapsed between said values assumed by the monitored signal set," as recited in exemplary Claim 12. Further, the setting of a total run time as a constraint during post-simulation analysis does not disclose "recording trace data ... within the trace array during the running of the testcase," as claimed. Consequently, the combination of *Raimi* and *Levin* does not render exemplary Claim 12, similar Claims 27 and 42, or their respective dependent claims unpatentable under 35 U.S.C. § 103.

B. Combination of *Raimi* and *Levin* does not disclose each feature recited in exemplary dependent Claim 52

The final rejection of exemplary dependent Claim 52 under 35 U.S.C. § 103 should also be reversed because the combination of *Raimi* and *Levin* does not disclose each feature of exemplary Claim 52 and, in particular, does not disclose:

> ... exporting the trace data in a trace file indicating an association between a value of said monitored signal set and an enumerated value containing a textual string.

In the Final Office Action, Claim 52 is rejected based upon a position advanced in the Advisory Action dated May 24, 2007, which argues that the instrumentation code set forth at col. 10, lines 48-51 of *Raimi* discloses the claimed "exporting" step. While Appellants agree that the disclosed instrumentation code includes the assignment of an integer value to a variable to record the results of a check of a logical AND operation, the mere disclosure of the assignment of an integer value to a variable by instrumentation logic as taught by *Raimi* does not establish a *prima facie* case that the combination *of Raimi* and *Levin* discloses that a trace file indicates "an association between a value of said monitored signal set and an enumerated value containing a textual string," as claimed. Consequently, the combination of *Raimi* and *Levin* does not render exemplary Claim 52 or similar Claims 66 and 80 unpatentable under 35 U.S.C. § 103.

C. Combination of *Raimi* and *Levin* does not disclose each feature recited in exemplary Claim 54

The final rejection of exemplary dependent Claim 54 under 35 U.S.C. § 103 should also be reversed because the combination of *Raimi* and *Levin* does not disclose each feature of exemplary Claim 54 and, in particular, does not disclose:

> the trace array has a counter that counts the functional cycles; and
> said recording trace data includes recording in the trace array an entry indicating overflow of said counter.

With respect to the above features, the Final Office Action cites col. 6, lines 13-22 of *Levin*, which disclose:

> As previously stated, event-sampling rates may be controlled by limiting the recording of event information to every Nth event. This is useful in cutting down the amount of data to be collected for cases where information integrity is not seriously disturbed by such data loss, such as the "instruction first cycle" (IFC), for example N might be 5 to 7 if the other sampled data of interest is happening frequently enough; and for branch events, N might be 2.

While the cited teaching of the combination *of Raimi* and *Levin* discloses an event counter, the cited teaching of the combination of *Raimi* and *Levin* does not disclose a functional cycle counter as claimed or recording an entry in a trace array indicating a counter overflow as claimed. Consequently, the combination of *Raimi* and *Levin* does not render exemplary Claim 54 or similar Claims 68 and 82 unpatentable under 35 U.S.C. § 103.

II. REJECTION OF CLAIMS 56, 58, 70, 72, 84 AND 86 UNDER 35 U.S.C. 103

In paragraph 9 of the Final Office Action, the final rejection of Claims 56, 58, 70, 72, 84 and 86 are rejected under 35 U.S.C. 103(a) as unpatentable over *Raimi* in view of *Levin* and further in view of the Examiner's Official Notice. That rejection is not well founded and should be reversed.

The final rejection of Claims 56, 58, 70, 72, 84 and 86 under 35 U.S.C. 103(a) as unpatentable over *Raimi* in view of *Levin* and further in view of the Examiner's Official Notice should be reversed because the Examiner has failed to establish a *prima facie* case of obviousness. In paragraph 9 of the Final Office Action, the Examiner states that he is taking Official Notice of features of Claim 56 as follows:

> File headers are routinely used and common place in file [sic] to identify the file and how it is to be opened. The file headers identify which program and the version of the program that was used in order to properly read the contents of the file. For example, MS Office version 2003 have [sic] a different header having a file version, than ones from, for example, MS Office 2000. It would have been obvious to do this because as technology advances there is a need to keep a certain amount of backward compatibility with legacy/old programs such that work does not need to be re-done with every version upgrade.

The Examiner then proceeds to take Official Notice of the features recited in Claim 58.

In response to the Examiner's assertion of Official Notice, first made in the non-final Office Action of January 10, 2008, Appellants seasonably traversed the Examiner's Official Notice in Amendment D, filed April 10, 2003. As clearly stated in MPEP 2144.03:

> It would not be appropriate for the examiner to take official notice of facts without citing a prior art reference where the facts asserted to be well known are not capable of instant and unquestionable demonstration as being well-known. For example, assertions of technical facts in the areas of esoteric technology or specific knowledge of the prior art must always be supported by citation to some reference work recognized as standard in the pertinent art. *In re Ahlert*, 424 F.2d at 1091, 165 USPQ at 420-21.

Accordingly, Appellants traversed the specific technical features relied upon by the Examiner, namely, specific MS Office and other software file formats, as not well-known. As further indicated in heading C of MPEP 2144.03, "If Applicant Challenges a Factual Assertion as Not Properly Officially Noticed or Not Properly Based Upon Common Knowledge, the Examiner Must Support the Finding With Adequate Evidence." In this case, the Examiner has not done so, but has merely asserted that Appellants traversal is "inadequate" when in fact the Examiner has failed to meet his burden of proof by supporting his unsupported assertions with documentary evidence.

Because the Examiner's Official Notice has been seasonably challenged and remains unsupported by documentary evidence, the Examiner has failed to establish a *prima facie* case of obviousness with respect to Claims 56, 58, 70, 72, 84 and 86, and the rejection under 35 U.S.C. § 103 should be reversed.

III. REJECTION OF CLAIMS 57, 71 AND 85 UNDER 35 U.S.C. 103

The final rejection of exemplary dependent Claims 57, 71 and 85 under 35 U.S.C. § 103 should also be reversed because the combination of *Raimi, Levin* and *Fomenko* does not disclose each feature of exemplary Claim 57 and, in particular, does not disclose:

> for each of a plurality of simulation runs, grouping all trace files from that simulation run in a respective one of a plurality of file system subdirectories that are each dedicated to one of the plurality of simulation runs.

In paragraph 10 of the Final Office Action, the Examiner cites paragraph [0024] of *Fomenko* as disclosing the features of Claim 57. In relevant part, the cited paragraph discloses:

> The Copy-Modify-Merge model is employed, for example, by Forte ™ TeamWare, available from Sun Microsystems, Inc. of Palo Alto, Calif. In accordance with this model, the data with which a software development team works is organized into files ("documents") and directories ("folders"). The files are placed in a special directory called a workspace. A workspace is a specially designated directory and its subdirectories. The workspace is called the "parent," and holds the master copy of all files ("master files"). Individual team members create their own workspace ("child" workspace) by copying the parent workspace ("bringover"). A child workspace is an exact copy of the current muster files in the parent workspace, and inherent all characteristics of the parent workspace. The individual team members work on their own copies of the files in the child workspace, and update them. Updating includes addition, deletion, and renaming of files. When the team member finish updating the files in the child workspace, the updated files are copied to the parent workspace, replacing the old files with the new ones ("putback").

The foregoing passage of *Fomenko*, taken in combination with *Raimi* and *Levin*, fails to disclose "a plurality of file system subdirectories that are each dedicated to one of the plurality of simulation runs," as claimed. Instead, the combination of references teaches establishing a redundant copy of a workspace for each of a plurality of users.

Because the combination of references does not disclose each feature of exemplary Claim 57, the rejection of Claim 56 and similar Claims 71 and 85 unpatentable under 35 U.S.C. § 103 should be reversed.

IV. CONCLUSION

The foregoing arguments demonstrate that the prior art of record does not disclose or render obvious each feature of the pending claims as required to support a rejection under 35 U.S.C. § 103. Appellants therefore respectfully request the Board to reverse the rejection of each pending claim.

No additional fee is believed to be required. If, however, any additional fees are required, please charge those fees to IBM Corporation Deposit Account No. **09-0447**.

Respectfully submitted,

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CLAIMS APPENDIX

1.-11. (canceled)

12. A method of reporting simulation data obtained by the simulation of an electronic design within a data processing system, said method comprising:

a simulator running a testcase against a simulation model of the electronic design, wherein:

the simulation model is formed of representations of instances of a plurality of design entities,

the instances of the design entities contain a plurality of signals and functional logic that define functional operation of the electronic design,

each instance of at least a particular design entity of the plurality of design entities contains an instance of an instrumentation entity that monitors the containing instance of the particular design entity but does not contribute to functional operation of the electronic design, and

each instance of the instrumentation entity contains a trace array logically coupled to receive a monitored signal set including at least one signal among the plurality of signals, wherein the trace array is further logically coupled to receive a control signal among the plurality of signals;

recording trace data for the monitored signal set within the trace array during the running of the testcase, wherein the recording includes concurrently storing within the trace array multiple values of the monitored signal set obtained over multiple cycles of functional operation of the simulation model, wherein recording trace data includes:

recording, within the trace array, values assumed by the monitored signal set during only those cycles of functional operation during which the control signal is asserted and refraining from recording values assumed by the monitored signal set during those cycles of functional operation during which the control signal is not asserted, such that no values assumed by the monitored signal set are recorded for those cycles of functional operation during which the control signal is not asserted; and

recording within the trace array a number of functional cycles elapsed between said values assumed by the monitored signal set;

exporting said trace data from said trace array in a trace file and storing said trace file in data storage.

13.-26. (canceled)

27. A data processing system, comprising:

means for running a testcase against a simulation model of an electronic design, wherein:

the simulation model is formed of representations of instances of a plurality of design entities,

the instances of the design entities contain a plurality of signals and functional logic that define functional operation of the electronic design,

each instance of at least a particular design entity of the plurality of design entities contains an instance of an instrumentation entity that monitors the containing instance of the particular design entity but does not contribute to functional operation of the electronic design, and

each instance of the instrumentation entity contains a trace array logically coupled to receive a monitored signal set including at least one signal among the plurality of signals, wherein the trace array is further logically coupled to receive a control signal among the plurality of signals;

means for recording trace data for the monitored signal set within the trace array during the running of the testcase, wherein the recording includes concurrently storing within the trace array multiple values of the monitored signal set obtained over multiple cycles of functional operation of the simulation model, wherein the means for recording trace data includes:

means for recording, within the trace array, values assumed by the monitored signal set during only those cycles of functional operation during which the control signal is asserted and for refraining from recording values assumed by the monitored signal set during those cycles of functional operation during which the control signal is not asserted, such that no values assumed by the monitored signal set are recorded for those cycles of functional operation during which the control signal is not asserted;

means for recording in the trace array a number of functional cycles elapsed between said values assumed by the monitored signal set; and

means for exporting said trace data from said trace array in a trace file and storing said trace file in data storage.

28.-41. (canceled)

42. An apparatus comprising:

a computer usable medium containing program code, said program code including:

instructions for running a testcase against a simulation model of an electronic design, wherein:

the simulation model is formed of representations of instances of a plurality of design entities,

the instances of the design entities contain a plurality of signals and functional logic that define functional operation of the electronic design,

each instance of at least a particular design entity of the plurality of design entities contains an instance of an instrumentation entity that monitors the containing instance of the particular design entity but does not contribute to functional operation of the electronic design, and

each instance of the instrumentation entity contains a trace array logically coupled to receive a monitored signal set including at least one signal among the plurality of signals, wherein the trace array is further logically coupled to receive a control signal among the plurality of signals; and

instructions for recording trace data for the monitored signal set within the trace array during the running of the testcase, wherein the recording includes concurrently storing within the trace array multiple values of the monitored signal set obtained over multiple cycles of functional operation of the simulation model, wherein the instructions for recording trace data include:

instructions for recording, within the trace array, values assumed by the monitored signal set during only those cycles of functional operation during which the control signal is asserted and for refraining from recording values

assumed by the monitored signal set during those cycles of functional operation during which the control signal is not asserted, such that no values assumed by the monitored signal set are recorded for those cycles of functional operation during which the control signal is not asserted;

instructions for recording in the trace array a number of functional cycles elapsed between said values assumed by the monitored signal set; and

instructions for exporting said trace data from said trace array in a trace file and storing said trace file in data storage.

43.-51. (canceled)

52. The method of Claim 12, wherein exporting the trace data in a trace file includes exporting the trace data in a trace file indicating an association between a value of said monitored signal set and an enumerated value containing a textual string.

53. (canceled)

54. The method of Claim 12, wherein:

the trace array has a counter that counts the functional cycles; and

said recording trace data includes recording in the trace array an entry indicating overflow of said counter.

55. The method of Claim 12, and further comprising:

during functional operation, the instrumentation entity signaling that the trace array is full;

in response to said signaling, automatically halting running of the testcase prior to completion of the testcase and performing said exporting; and

thereafter, resuming running of the testcase.

56. The method of Claim 12, wherein said exporting includes:

exporting a trace file including a plurality of fields, said plurality of fields including at least one of a set comprising a file version field and an array type field indicating one of plurality of trace array types.

57. The method of Claim 12, wherein said storing comprises:

for each of a plurality of simulation runs, grouping all trace files from that simulation run in a respective one of a plurality of file system subdirectories that are each dedicated to one of the plurality of simulation runs.

58. The method of Claim 12, wherein said storing comprises automatically naming the trace file in data storage by a filename indicating the containing instance of the particular design entity.

59. The method of Claim 12, and further comprising accessing the trace file in data storage with a trace analysis tool.

60.-65. (canceled)

66. The data processing system of Claim 27, wherein said means for exporting the trace data in a trace file includes means for exporting the trace data in a trace file indicating an association between a value of said monitored signal set and an enumerated value containing a textual string.

67. (canceled)

68. The data processing system of Claim 27, wherein:

the trace array has a counter that counts the functional cycles; and

said means for recording trace data includes means for recording in the trace array an entry indicating overflow of said counter.

69. The data processing system of Claim 27, and further comprising:

means for detecting signaling by the instrumentation entity during functional operation that the trace array is full;

means, responsive to said signaling, for automatically halting running of the testcase prior to completion of the testcase; and

means for resuming running of the testcase after exporting said trace data.

70. The data processing system of Claim 27, wherein said means for exporting includes:

means for exporting a trace file including a plurality of fields, said plurality of fields including at least one of a set comprising a file version field and an array type field indicating one of plurality of trace array types.

71. The data processing system of Claim 27, wherein said means for storing comprises:

means, for each of a plurality of simulation runs, for grouping all trace files from that simulation run in a respective one of a plurality of file system subdirectories that are each dedicated to one of the plurality of simulation runs.

72. The data processing system of Claim 27, wherein said means for storing comprises means for automatically naming the trace file in data storage by a filename indicating the containing instance of the particular design entity.

73. The data processing system of Claim 27, and further comprising a trace analysis tool for accessing the trace file in data storage.

74.-79. (canceled)

80. The apparatus of Claim 42, wherein the instructions for exporting the trace data in a trace file include instructions for exporting the trace data in a trace file indicating an association between a value of said monitored signal set and an enumerated value containing a textual string.

81. (canceled)

82. The apparatus of Claim 42, wherein:

the trace array has a counter that counts the functional cycles; and

said instructions for recording trace data include instructions for recording in the trace array an entry indicating overflow of said counter.

83. The apparatus of Claim 42, and further comprising:

instructions for detecting signaling during functional operation by the instruction entity that the trace array is full;

instructions, in response to said signaling, for automatically halting running of the testcase prior to completion of the testcase and performing said exporting; and

thereafter, resuming running of the testcase.

84. The apparatus of Claim 42, wherein said instructions for exporting include:

instructions for exporting a trace file including a plurality of fields, said plurality of fields including at least one of a set comprising a file version field and an array type field indicating one of plurality of trace array types.

85. The apparatus of Claim 42, wherein said instructions for storing comprise:

instructions that, for each of a plurality of simulation runs, group all trace files from that simulation run in a respective one of a plurality of file system subdirectories that are each dedicated to one of the plurality of simulation runs.

86. The apparatus of Claim 42, wherein said instructions for storing comprises instructions for automatically naming the trace file in data storage by a filename indicating the containing instance of the particular design entity.

87. The apparatus of Claim 42, and further comprising a trace analysis tool for accessing the trace file in data storage.

EVIDENCE APPENDIX

none

RELATED PROCEEDINGS APPENDIX

none